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HEWLETT-PACKARD COMPANY
Intellectual Property Administration
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PATENT APPLICATION

ATTORNEY DOCKET NO. 10002861 -1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Zhizhang Chen et al **Confirmation No.:** 9286

Application No.: 09/817703 **Examiner:** Foong

Filing Date: Mar 26, 2001 **Group Art Unit:** 2853

Title: LDMOS And CMOS Integrated Circuit And Method Of Making

COMMISSIONER FOR PATENTS
Washington, D.C. 20231

TRANSMITTAL LETTER FOR RESPONSE/AMENDMENT

Sir:

Transmitted herewith is/are the following in the above-identified application:

(X) Response/Amendment ( ) Petition to extend time to respond
( ) New fee as calculated below ( ) Supplemental Declaration
(X) No additional fee (Address envelope to "Box Non-Fee Amendments")
( ) Other: _____ (fee $_____)

CLAIMS AS AMENDED BY OTHER THAN A SMALL ENTITY						
(1) FOR	(2) CLAIMS REMAINING AFTER AMENDMENT	(3) NUMBER EXTRA	(4) HIGHEST NUMBER PREVIOUSLY PAID FOR	(5) PRESENT EXTRA	(6) RATE	(7) ADDITIONAL FEES
TOTAL CLAIMS		MINUS		= 0	X $18	$ 0
INDEP. CLAIMS		MINUS		= 0	X $84	$ 0
[ ] FIRST PRESENTATION OF A MULTIPLE DEPENDENT CLAIM					+ $280	$ 0
EXTENSION FEE	1ST MONTH $110.00 [ ]	2ND MONTH $410.00 [ ]	3RD MONTH $930.00 [ ]	4TH MONTH $1450.00 [ ]		$ 0
					OTHER FEES	$
					TOTAL ADDITIONAL FEE FOR THIS AMENDMENT	$ 0

Charge $ 0 to Deposit Account 08-2025. At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. ~~A duplicate copy of this sheet is enclosed~~.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231.

Date of Deposit: 2/19/03

Typed Name: **Timothy F. Myers**

Signature: Timothy F. Myers

Respectfully submitted,

Zhizhang Chen et al

By Timothy F. Myers

Timothy F. Myers

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Rev 02/03 (TransAmd)

- Attach as First Page to Transmitted Papers -

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE #9/Amdt A AR Dawd 3/3/03

In re application of: Z. Chen et al. Art Unit: 2853
Examiner: Foong, Suk San

Serial Number: 09/817,703
Filed: March 26, 2001
Title: LDMOS AND CMOS INTEGRATED CIRCUIT AND METHOD OF MAKING
Date: 2/19/03

AMENDMENT UNDER 37 CFR § 1.111

TO THE ASSISTANT COMMISSIONER FOR PATENTS:

Sir:

In response to the Office Action dated December 4, 2002, please amend the above-identified patent application as follows:

In the Specification:

Please replace the paragraph starting on page 8, line 21 with the following:

Figs. 4A and 4B make up an exemplary flow chart of a modified semiconductor process embodying the invention. Figs 5A through 5M are cross-sectional views of exemplary and some excluded process steps on a substrate 10. The step 50 of Fig. 3A of creating a defined deposition of a first dielectric layer 124 to expose a first region 20 and a second region 22, is illustrated in Fig. 5A. The first dielectric layer 124 can be made of one or more conventional thin film dielectrics. An exemplary first dielectric layer is made up of 200 Angstroms of SRO (stress relief oxide) and 900 Angstroms of silicon nitride. The process step 52 of Fig. 3A can be performed to provide the selective doping of the well regions with essentially the following steps. As shown in Fig 5B and in step 60 of Fig. 4A, a first conductivity dopant of impurities [126]128 is implanted into the first and